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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,015	11/17/2003	Jang-Won Moon	5649-1098	3312

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/715,015	MOON ET AL.
	Examiner	Art Unit
	Jung (John) Hur	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,15 and 16* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 23 September 2005. The changes and remarks disclosed therein have been considered.

Claims 2 and 3 have been cancelled by Amendment. Therefore, claims 1 and 4-16 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 22 June 2005. The information disclosed therein has been considered.

Specification

3. Claim 1 is objected to because of the following informalities:

In claim 1, lines 10-11 and 12, "the column address bank signal" should be --the column bank address signal--, and in lines 14-15, "a second precharge signal" should be --a second precharge control signal--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-7, 9, 10, 15 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art ("Admission") in view of Yu et al. (U.S. Pat. No. 5,828,612).

Admission, in Figs. 1A and 1B, discloses a memory device, and a related method, comprising: a pair of data input/output lines (see for example page 1, line 14 of the instant specification); a delay precharge circuit (1000); a column bank address signal (CBA); a write enable signal (inherent); a precharge circuit (including a PMOS transistor; see page 1, line 12); a precharge control signal (PIOPRB); a first delayed signal (related to the output of 10); a first precharge control signal (related to the output of 15) rising in synchronization with a rising edge of the column bank address signal and falling a first predetermined time period (related to the delay of 10) after an immediately succeeding falling edge of the column bank address signal (see Fig. 1B); precharging after the first predetermined time period following assertion of the column bank address signal when the write enable signal indicates a read operation (see for example page 2, lines 17-19); the precharge delay control circuit causing application of the first precharge control signal after a read operation (see for example page 2, lines 17-19).

Admission does not disclose a second precharge control signal rising in synchronization with the rising edge of the column bank address signal and falling a second predetermined time period after an immediately succeeding falling edge of the column bank address signal; precharging after the second predetermined time period following assertion of the column bank address signal when the write enable signal indicates a write operation; the precharge delay control circuit causing application of the second precharge control signal after a write operation; selecting one of the first precharge control signal and the second precharge control signal based

on a state of the write enable signal; and the first predetermined time period being greater than the second predetermined time period.

However, Yu, for example in Fig. 3, discloses a first precharge control signal (see /PRECHARGE 110 in Fig. 3, related to a READ operation) with a first predetermined time period (related to t2); a second precharge control signal (see /PRECHARGE 110 in Fig. 3, related to a WRITE operation) with a second predetermined time period (related to t5); the second predetermined time period being shorter than the first predetermined time period (see Fig. 3); a write enable signal (R/W 102); and selecting the first precharge control signal for a write operation and the second precharge control signal for a read operation, based on the state of the write enable signal (see /PRECHARGE 110 in Fig. 3).

In view of Yu's teaching of the advantages of having different and independently optimized precharge delay depending on the type of access operation (see for example Yu, column 2, lines 36-41), it would have been obvious at the time the invention was made to a person having ordinary skill in the art, who is familiar with Admission, to modify the device and the related method of Admission to generate a second precharge control signal responsive to the bank address signal (in a manner similar to that of Fig. 1A of Admission, but with a shorter delay than that of the first precharge control signal), and to select the first precharge control signal for a read operation and the second precharge control signal for a write operation, determined by the write enable signal (for example, using a multiplexer, commonly used and well known in the art), for the purpose of increasing the frequency of operation (see, for example, Yu, column 2, lines 36-41).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of Yu et al. (U.S. Pat. No. 5,828,612) as applied to claim 6 above, and further in view of Nitta et al. (U.S. Pat. No. 5,831,924).

The above Admission/Yu combination discloses a memory device as recited in claim 6, with the exception of the pair of data input/output lines being a pair of global input/output lines. Nitta discloses a pair of global input/output lines that are precharged (see for example column 3, lines 37-42). Since memories having a pair of global input/output lines that are precharged were common and well known in the art (as exemplified by Nitta), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the precharging means of the Admission/Yu combination to such memories, for the purpose of increasing the frequency of operation in such memories (see for example Yu, column 2, lines 36-41).

Allowable Subject Matter

7. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The record of the prosecution as a whole makes clear the reasons for the indication of allowable subject matter.

Response to Arguments

8. Applicant's arguments filed 23 September 2005 have been fully considered but they are not persuasive.

Starting at the bottom of page 6, Applicant argues that neither Admission nor Yu discloses or suggests generation of first and second delayed signals from the column bank address signals, and generation of first and second precharge control signals from the first and second delayed signals, respectively.

In response, it is noted that the combination of Admission and Yu, as recited in the previous rejections repeated above, would include generation of first and second delayed signals from the column address bank signals, and generation of first and second precharge control signals from the first and second delayed signals, respectively.

Starting near the top of page 7, Applicant argues that "contrary to the assertion in the Office Action, Yu provides no suggestion to modify Admission to provide such features. In particular, the portions cited from Yu (see Office Action p. 4) merely indicate that it may be desirable to provide independent precharge timing for read and write operations, and that such different timing may [be] achieved responsive to a write enable signal. However, there is nothing in Yu that teaches or suggests, for example, how first and second delayed signals generated from a column bank address signal could be used to generate such different timings."

In response, it is noted that Yu, in the portions cited in the previous Office Action and repeated above, also discloses why it is desirable to have independent precharge timing for read and write operations (responsive to a write enable signal), thus motivating one of ordinary skill in the art to provide such desirable capabilities in the memory device of Admission.

Further, since Admission discloses a type of memory device that uses a column bank address signal to generate a precharge control signal with a delay, one of ordinary skill in the art,

in order to provide said desirable capabilities of Yu in such memory, would use a similar means (i.e., using the column bank address signal with a different delay) to generate a second precharge control signal, as recited in the previous rejections repeated above, thus generating different precharge timings for read and write operations.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER